Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.144”**

**SOURCE**

**G**

**.152”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Source: .040” X .060”**

**Gate: .020” X .023”**

**Backside Potential: DRAIN**

**Mask Ref: HEX 3, P-Channel**

**APPROVED BY: DK DIE SIZE .144” X .152” DATE: 7/17/23**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRFC9034B**

**DG 10.1.2**

#### Rev B, 7/19/02